REMARKS

Applicants respectfully request reconsideration of the above identified application. Claims 1-30 and 35-46 are pending. Claims 1-30 and 35-46 are rejected.

The remaining comments are directed to the rejected claims. Applicant respectfully notes that in the Office Action mailed on July 21, 2004, responses to Applicant's arguments of May 11, 2004; interpretations or characterizations by the Examiner, include inferences and/or potential limitations, to which Applicant does not agree. Being respectful of the Examiner's time, Applicant will address only issues necessary to traverse the Examiner's rejections and reserve the right to address such inferences and/or potential limitations in the future should the Examiner elect to rely upon them.

35 U.S.C. § 112 Rejections

The Office Action mailed on July 21, 2004 rejects Claims 1-30 and 35 under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. Applicant respectfully disagrees.

The Examiner states that the present application does not show how to make the identification of sharability of a translation transparent to the operating system.

But the present application states (p. 14-16, par. 37-40):

> Control logic 604 may use the data portion 614, sharing indication 619, and data portion 624 to identify if the virtual address translation is sharable. For example, if a processor initiates a TLB request to look up a virtual address translation and the TLB entry in latches 633 and 637 contains an ASID that matches the ASID for the virtual address to be translated, and further if the entry contains a VAD that matches the VAD for the virtual address, and finally if sharing indication 619 indicates a set of logical processes including one associated with the processor initiating the TLB request, then the entry in latch 633 and latch 637 may be used to translate the virtual address. Otherwise, control logic 604 may initiate installation of a new virtual address translation entry for TLB 602.
>
> Whenever a miss occurs in TLB 602, the physical address data and other TLB data may be recovered from page tables in main memory. For one alternative embodiment control logic 604 may comprise a mechanism for recovering such data. Most modern processors use a mechanism called a page walker to access page tables in memory and compute physical addresses on TLB misses.

If a processor, either directly through software or indirectly through control logic 604, initiates a TLB request to installation of a new virtual address translation entry, the TLB 602 may be searched for any existing entries that can be shared. An entry retrieved from tag array 631 and translation array 635 may then be latched by latch 633 and latch 637 respectively. If the TLB entry in latches 633 and 637 contains an ASID that matches the ASID for the virtual address to be translated, and further if the entry contains a VAD that matches the VAD for the virtual address, and finally if sharing indication 619 indicates a shared status, then the entry in latch 633 and latch 637 may be installed for the processor initiating the TLB request by adding the logical process associated with the initiating processor to the set of logical processes indicated by sharing indication 619 and thereafter the TLB entry may be used to translate the virtual address. Otherwise, control logic 604 may initiate allocation of a new virtual address translation entry for TLB 602.

If a processor, either directly through software or indirectly through control logic 604, initiates a TLB request to allocate a new virtual address translation entry, the TLB 602 may be searched for any invalid or replaceable entries. The retrieved TLB entry may then be reset by control logic 604 to contain an ASID that matches the ASID for the virtual address to be translated, a VAD that matches the VAD for the virtual address, a PAD that matches the PAD of the translated physical address, an ATRD that matches the ATRD of the translated physical address, and any other associated data corresponding to the virtual address translation. Finally the entry may be installed for the processor initiating the TLB allocation request by initializing the set of logical processes indicated by sharing indication 619 to contain only the logical process associated with the initiating processor. It will be appreciated that the sharing indication 619 may be conveniently initialized by default to indicate a shared status for the virtual address translation. Alternatively if the allocation was initiated through software, for example, control logic 604 may initialize the sharing indication 619 by default to indicate a private status for the virtual address translation.

It further states with regard to Fig. 7a (p. 19, par. 46-48):

In Figure 7a, for example, a sharing indication corresponding to virtual address translation entry 711 indicates a private status of P and a set of logical processes of 0001, the low order bit being set to indicate that entry 711 may be used exclusively to translate virtual addresses for processor 710. Similarly a sharing indication corresponding to virtual address translation entry 713 indicates a private status of P and a set of logical processes of 0100, indicating that entry 713 may be used exclusively to translate virtual addresses for processor 740.

A sharing indication corresponding to virtual address translation entry 712 indicates a shared status of S and a set of logical processes of 0101, indicating that entry 712 may be shared and may be used to translate virtual addresses for processors 710 and 740. Similarly a sharing indication corresponding to virtual address translation entry 719 indicates a shared status of S and a set of logical processes of 1111, indicating that entry 719 may be shared and used to translate virtual addresses for all four processors 710-780.

A sharing indication corresponding to virtual address translation entry 716 indicates a invalid status of I and a set of logical processes of 0000 meaning that entry 716 may not be used to translate virtual addresses for any processor 710-780. It will be appreciated that the invalid status may be explicitly represented or implicitly represented by the

corresponding set of logical processes. It will also be appreciated that one skilled in the art may produce other encodings to explicitly or implicitly represent sharing indications for TLB entries.

It further states with regard to Fig. 7b (p. 20, par. 49-50):

In Figure 7b, for example, a sharing indication corresponding to virtual address translation entry 711 may implicitly indicate a private status of P and an explicit set of logical processes of 01 meaning that entry 711 may be used to translate virtual addresses for processor 710. It will be appreciated that such an implicit status representation may permit any implicit private status to be changed to an implicit shared status if another processor is found that may make use of the corresponding virtual address translation entry.

For example, if a processor initiates a TLB request to look up a virtual address translation and the sharing indication corresponding to the retrieved TLB entry indicates a set of logical processes that does not include one associated with the processor initiating the TLB request, then the physical address data and other TLB data may be recovered from page tables in main memory. Control logic 704 may include a mechanism for recovering such data, or may invoke a mechanism such as a page walker to access page tables in memory and compute physical addresses. If the newly constructed virtual address translation matches the retrieved TLB entry, the requesting process may be added to the set of logical processes sharing the retrieved TLB entry. Otherwise the newly constructed virtual address translation may be installed in a new TLB entry for the requesting processor.

Therefore, Applicant respectfully submits that the present application discloses how to make the identification of sharability of a translation transparent to the operating system such that one skilled in the art may practice the entire scope of the subject matter claimed without undo experimentation. Therefore, Applicant respectfully requests the Examiner withdraw his rejections under 35 U.S.C. 112, first paragraph.

The Office Action also rejects Claims 1-30 and 35 under 35 U.S.C. 112, second paragraph, as allegedly failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully disagrees.

Applicant refers to a definition from McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, (attached) which defines:

transparent [COMPUT SCI] pertaining to a device or system that processes data without the user being aware of or needing to understand its operation.

Applicant respectfully submits that the limitation, "transparent to the operating system" is not indefinite, being composed of well known terms of art. Therefore, Applicant respectfully requests the Examiner withdraw his rejections under 35 U.S.C. 112, second paragraph.

35 U.S.C. § 102(e) Rejections

The Office Action rejects Claims 1-30 and 35-46 under 35 U.S.C. 102(e) as allegedly being anticipated by U.S. Patent 6,598,050 B1 (Bourekas).

Applicant respectfully disagrees with the Examiner's anticipation assertions.

Applicant argued in the appeal brief filed May 11, 2004 that the invention of Bourekas relates to a virtual addressing scheme within a microprocessor based system (col. 1, lines 8-9). In this virtual addressing scheme, the virtual addresses have a group membership field (col. 2, lines 27-28). The group membership field is used to permit sharing of data and/or programs among a subset of tasks in a multi-tasking system (col. 2, lines 21-23). With the use of the group membership field, the operating system can support three levels of access in a virtual to physical address translation. The operating system permits a global translation, an individual translation and a group translation," (col. 5, line 65 through col. 6, line 2, emphasis added).

In response to the above argument, the Examiner argues that neither this nor anything else in the reference requires the operating system to be modified as required by the apparent definition of "transparent" in the claims and that Bourekas does not disclose how the operating system was to be modified.

Applicant respectfully submits that when the operating system is not modified to support virtual addresses that have the group membership fields of Bourekas, there is no alternative method to permit shared translations, either expressly or inherently described. Whether Bourekas is enabling is not relevant to the issue at hand. The MPEP § 2131 states that:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claims 1, 9 and 35 set forth operating-system transparent methods that comprise accessing or installing a virtual address translation and transparently identifying if the virtual address translation is sharable or enabling sharing. Claims 13 and 20 both set forth apparatus to provide operating-system transparent sharing of virtual address

translations comprising control logic to transparently produce or provide a sharing indication if a virtual address translation may be shared.

Applicant respectfully submits that in the cited reference, each and every element as set forth in the independent claims 1, 9, 13, 20 and 35 is not found, either expressly or inherently described.

In the multithreading processor of claim 36, a control logic comprises circuitry to identify a sharability of a first TLB entry and to provide a first sharing indication to indicate if the first entry may be shared by a second process. Claim 36 further sets forth a sharing indication field in the first TLB entry to store the first sharing indication provided by the control logic.

Bourekas relates to a virtual addressing scheme wherein a group of tasks may be marked for access to a given translation (col. 1, lines 8-9; col. 3, lines 1-3). In Bourekas, both the global bit and the group membership field stored in the TLB entry come from the virtual address translation provided by the operating system (col. 5, line 65 through col. 6, lines 2 and lines 51-52)--not from processor control logic as set forth in claim 36. Matching circuitry of Bourekas receives static group membership fields from the virtual address and from the TLB and simply matches them to determine if they were marked as belonging to the same group (col. 7, line 60 through col. 8, line 2).

The MPEP § 2131 states that:

> "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant respectfully submits that Bourekas does not expressly or inherently describe, in as complete detail as is set forth by claim 36: a multithreading processor with control logic to identify sharability of a TLB entry, to provide a sharing indication to indicate if the first entry may be shared by another process and to store the sharing indication provided by the control logic in a field in the TLB entry.

Accordingly in light of the argument presented above, Applicant submits that independent claims 1, 9, 13, 20, 35 and 36 are not anticipated by Bourekas.

The Office Action also rejects Claims 1-30 and 35-46 under 35 U.S.C. 102(e) as allegedly being anticipated by U.S. Patent 6,564,311 B2 (Kakeda).

Applicant respectfully disagrees with the Examiner's anticipation assertions.

Kakeda relates to yet another virtual addressing scheme wherein a group of tasks may be marked for access to a given translation. With regard to Figures 4 and 5, Kakeda contrasts the conventional address translation using one global bit (Fig. 5) as compared with the two-global-bit embodiment of his invention (Fig. 4, col. 9, line 24 through col. 10 line 25). He discloses that his global bits are the "comparison information" (col. 2, lines 53-62) and describes how process identifiers (col. 8, lines 13-43) and global bits must be set (col. 8, line 48 through col. 9, line 13). The apparatus of Kakeda is specific to the addressing scheme described and therefore the establishment of page tables (col. 12, line 49, and Fig. 4) to take advantage of Kakeda is not operating-system transparent.

Accordingly in light of the argument presented above, Applicant respectfully submits that in the cited reference, each and every element as set forth in the independent claims 1, 9, 13, 20 and 35 is not found, either expressly or inherently described.

As stated above with regard to claim 36, a control logic comprises circuitry to identify a sharability, to provide a first sharing indication to indicate if the first entry may be shared by a second process and a sharing indication field in the first TLB entry stores the first sharing indication provided by the control logic.

With regard to the comparators 13 and the AND gates 105, Kakeda does not disclose providing a first sharing indication to indicate if the first entry may be shared by a second process as argued by the Examiner. Further, Kakeda does not disclose that what comparators 13 and AND gates 105 do provide is stored in process identifier storage area 102 or that what is stored in process identifier storage area 102 is provided by comparators 13 and AND gates 105 as argued by the Examiner (col. 5, line 66 through col. 6, line 34, and Figs. 1-2).

Accordingly in light of the argument presented above, Applicant submits that independent claims 1, 9, 13, 20, 35 and 36 are not anticipated by Kakeda.

CONCLUSION

Applicants respectfully submit the present claims for allowance.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence Mennemeier at (408) 765-2194.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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...e range just above and just below the acoustic velocity. { tran'sän·ik 'flō }

...nsonic range [FL MECH] The range of speeds between the speed at which one point on a body reaches supersonic speed, and the speed at which all points reach supersonic speed. { tran'sän·ik 'rānj }

...nsonic speed [FL MECH] The speed of a body relative to the surrounding fluid at which the flow is in some places on the body subsonic and in other places supersonic. { tran'sän·ik 'spēd }

...nsonic wind tunnel [ENG] A type of high-speed wind tunnel capable of testing the effects of airflow past an object at speeds near the speed of sound, Mach 0.7 to 1.4; sonic speed occurs where the cross section of the tunnel is at a minimum, that is, where the test object is located. { tran'sän·ik 'wind ,tən·əl }

...nsorbital lobotomy [MED] A lobotomy performed through the roof of the orbit. { tranz'ȯr·bəd·əl lə'bäd·ə·mē }

...nsosonde [ENG] The flight of a constant-level balloon, whose trajectory is determined by tracking with radio-direction-finding equipment; thus, it is a form of upper-air, quasi-horizontal sounding. { 'tran·zə,sänd }

...nsparency [GRAPHICS] An image fixed on a clear base by means of a photographic, printing, chemical, or other process, especially adaptable for viewing by transmitted light. [OPTICS] The ability of a substance to transmit light of different wavelengths, sometimes measured in percent of radiation which penetrates a distance of 1 meter. { tranz'par·ən·sē }

...nsparency range [NUC PHYS] A postulated energy range for extremely high-energy heavy-ion collisions in which the projectile passes through the target and emerges with its temperature and density raised to the point at which a quark-gluon plasma forms. { tranz'par·ən·sē ,rānj }

...nsparent [COMPUT SCI] Pertaining to a device or system that processes data without the user being aware of or needing to understand its operation. [PHYS] Permitting passage of radiation or particles. { tranz'par·ənt }

...nsparent medium [OPTICS] **1.** A medium which has the property of transmitting rays of light in such a way that the human eye may see through the medium distinctly. **2.** A medium transparent to other regions of the electromagnetic spectrum, such as x-rays and microwaves. { tranz'par·ənt 'mēd·ē·əm }

...nsparent sky cover [METEOROL] In United States weather-observing practice, that portion of sky cover through which higher clouds and blue sky may be observed; opposed to opaque sky cover. { tranz'par·ənt 'skī ,kəv·ər }

...nspassive region [PHYS CHEM] That portion of an anodic polarization curve in which metal dissolution increases as the potential becomes noble. { tranz'pas·iv ,rē·jən }

...nsphasor [OPTICS] A nonlinear optical device that uses one light beam to modulate another, in a manner analogous to an electronic transistor, and that operates through the transference of a phase shift from one beam to the other. { ,tranz 'fāz·ər }

...nspiration [BIOL] The passage of a gas or liquid (in the form of vapor) through the skin, a membrane, or other tissue. { ,tranz·pə'rā·shən }

...nspiration cooling *See* sweat cooling. { ,tranz·pə'rā·shən ,kül·iŋ }

...nsplantation [BIOL] **1.** The artificial removal of part of an organism and its replacement in the body of the same or of a different individual. **2.** To remove a plant from one location and replant it in another place. { ,tranz·plan'tā·shən }

...nsplantation antigen [IMMUNOL] An antigen in a cell which induces a histocompatibility reaction when the cell is transplanted into an organism not having that antigen. { ,tranz·plan'tā·shən 'ant·i·jən }

...nsplantation disease [MED] Disease ascribable to an immunological graft-versus-host reaction which occurs after transplantation of adult lymphoid cells to incompatible recipients who cannot reject them. { ,tranz·plan'tā·shən di,zēz }

...nsplanter [AGR] A special kind of equipment designed for the planting of cuttings or small plants; it transports one or more workers who assist the action of the machine in placing plants in a furrow and covering them; it commonly supplies a small quantity of water to each plant. { tranz'plan·tər }

...nsplutonium element [INORG CHEM] An element having an atomic number greater than that of plutonium (94). { ,tranz·plə'tō·nē·əm 'el·ə·mənt }

transpolarizer [ELEC] An electrostatically controlled circuit impedance that can have about 30 discrete and reproducible impedance values: two capacitors, each having a crystalline ferroelectric dielectric with a nearly rectangular hysteresis loop, are connected in series and act as a single low impedance to an alternating-current sensing signal when both capacitors are polarized in the same direction; application of 1-microsecond pulses of appropriate polarity increases the impedance in steps. { tranz'pō·lə,rīz·ər }

transponder [COMMUN] **1.** A transmitter-receiver capable of accepting the challenge of an interrogator and automatically transmitting an appropriate reply. **2.** A receiver-transmitter, such as on satellites, which receives a transmission and retransmits it at another radio frequency. { tranz'pän·dər }

transponder beacon *See* responder beacon. { tranz'pän·dər ,bē·kən }

transponder dead time [ELECTR] Time interval between the start of a pulse and the earliest instant at which a new pulse can be received or produced by a transponder. { tranz'pän·dər 'ded ,tīm }

transponder set [ELECTR] A complete electronic set which is designed to receive an interrogation signal, and which retransmits coded signals that can be interpreted by the interrogating station; it may also utilize the received signal for actuation of additional equipment such as local indicators or servo amplifiers. { tranz'pän·dər ,set }

transponder suppressed time delay [ELECTR] Overall fixed time delay between reception of an interrogation and transmission of a reply to this interrogation. { tranz'pän·dər sə'prest 'tīm di,lā }

transport [COMPUT SCI] **1.** To convey as a whole from one storage device to another in a digital computer. **2.** *See* tape transport. [ENG] Conveyance equipment such as vehicular transport, hydraulic transport, and conveyor-belt setups. [NAV ARCH] A ship designed to carry military personnel from one place to another. Also known as troop ship. { trans'pȯrt (verb), 'tranz,pȯrt (noun) }

transportable computer [COMPUT SCI] A microcomputer that can be carried about conveniently but, in contrast to a portable computer, requires an external power source. { tranz'pȯrd·ə·bəl kəm'pyüd·ər }

transportation [GEOL] A phase of sedimentation concerned with movement by natural agents of sediment or any loose or weathered material from one place to another. { ,tranz·pər'tā·shən }

transportation emergency [ENG] A situation which is created by a shortage of normal transportation capability and of a magnitude sufficient to frustrate movement requirements, and which requires extraordinary action by the designated authority to ensure continued movement. { ,tranz·pər'tā·shən i,mər·jən·sē }

transportation engineering [ENG] That branch of engineering relating to the movement of goods and people; major types of transportation are highway, water, rail, subway, air, and pipeline. { ,tranz·pər'tā·shən ,en·jə,nir·iŋ }

transportation lag *See* distance/velocity lag. { ,tranz·pər'tā·shən ,lag }

transportation priorities [ENG] Indicators assigned to eligible traffic which establish its movement precedence; appropriate priority systems apply to the movement of traffic by sea and air. { ,tranz·pər'tā·shən prī,är·əd·ēz }

transportation problem [IND ENG] A programming problem that is concerned with the optimal pattern of the distribution of goods from several points of origin to several different destinations, with the specified requirements at each destination. { ,tranz·pər'tā·shən ,präb·ləm }

transport capacity [ENG] The number of persons or the tonnage (or volume) of equipment which can be carried by a vehicle under given conditions. { 'tranz,pȯrt kə,pas·əd·ē }

transport case [ENG] A moistureproof nonconductive wood, plastic, or fabric container used to transport safely small quantities of dynamite sticks to and from blasting sites. { 'tranz,pȯrt ,kās }

transport cross section [PHYS] The product of the total scattering cross section and the average value of $1 - \cos\theta$, where θ is the laboratory scattering angle. { 'tranz,pȯrt 'krȯs ,sek·shən }